What Is Claimed Is:

1. An apparatus for applying a desired voltage at a first node, said first node being connected to a load impedance, said apparatus comprising:

a voltage source coupled to said first node, said voltage source generating said desired voltage; and

a current source also coupled to said first node, wherein said current source supplies an amount of current that would be approximately drawn by said load impedance if said desired voltage were to be applied at said first node.

2. The apparatus of claim 1, wherein said load impedance is characterized by a high load such that said current source enables said voltage source to be coupled to said first node without a buffer between said voltage source and said first node.

3. The apparatus of claim 1, wherein said desired voltage is to be applied to a plurality of nodes including said first node, said plurality of nodes being connected in series with a corresponding routing resistance present between each pair of said plurality of nodes, each of said plurality of nodes being connected to a corresponding one of a plurality of load impedances, said apparatus further comprising:

a plurality of current sources, each of said plurality of current sources being coupled to a corresponding one of said plurality of nodes, each of said plurality of current sources supplying an amount of current approximately equal to said desired voltage divided by a load impedance driven by the corresponding coupled node, said plurality of current sources comprising said current source.

4. The apparatus of claim 3, wherein said current source comprises a resistor having a resistance equal to said load impedance.

5. An analog to digital converter (ADC) converting a sample of an analog signal to a digital code, said ADC comprising:

a plurality of stages, each of said plurality of stages generating a corresponding one of a plurality of sub-codes, each of said plurality of sub-codes containing at least one bit, wherein said sub-codes are used to generate said digital code, each of said plurality of stages comprising:

a resistor ladder having a first end and a second end, said first end of said resistor ladder being coupled to a voltage source providing a desired voltage, the first end of all of the resistor ladders being connected in series, said first end of said resistor ladder also being coupled to a current source, said current source supplying to said resistor ladder an amount of current approximately equal to said desired voltage divided by an impedance offered by said resistor ladder.

6. The ADC of claim 5, wherein each of said plurality of stages further comprising:

a sub-ADC receiving an input signal and a reference voltage, said sub-ADC generating a corresponding one of said plurality of sub-codes;

a digital to analog converter (DAC) converting said corresponding one of said plurality of sub-codes into a corresponding intermediate voltage according to said reference voltage;

a subtractor subtracting said corresponding intermediate voltage from said input signal to generate a subtractor output; and

an amplifier amplifying said subtractor output to generate said input signal for a next one of said plurality of stages, wherein said sample is provided as said input signal for the first one of said plurality of stages.

7. The ADC of claim 6, wherein said sub-ADC comprises said resistor ladder and said current source

8. The ADC of claim 6, wherein said voltage source provides a reference voltage for said ADC.

9. The ADC of claim 6, wherein said ADC operates in a differential mode.

10. The ADC of claim 6, wherein said ADC operates in a single-ended mode.

11. A device processing an analog signal, said device comprising:

a voltage source providing a reference voltage;

a current source;

an analog to digital converter (ADC) converting a sample of said analog signal to a digital code, said ADC comprising:

a plurality of stages, each of said plurality of stages generating a corresponding one of a plurality of sub-codes, each of said plurality of sub-codes containing at least

one bit, wherein said sub-codes are used to generate said digital code, each of said plurality of stages comprising:

a resistor ladder having a first end and a second end, said first end of said resistor ladder being coupled to said voltage source providing said reference voltage, the first end of all of the resistor ladders being connected in series, said first end of said resistor ladder also being coupled to said current source,

said current source supplying to said resistor ladder an amount of current approximately equal to said desired voltage divided by an impedance offered by said resistor ladder; and

a processing block receiving said digital code.

12. The device of claim 11, wherein each of said plurality of stages further comprising:

a sub-ADC receiving an input signal and a reference voltage, said sub-ADC generating a corresponding one of said plurality of sub-codes;

a digital to analog converter (DAC) converting said corresponding one of said plurality of sub-codes into a corresponding intermediate voltage according to said reference voltage;

a subtractor subtracting said corresponding intermediate voltage from said input signal to generate a subtractor output; and

an amplifier amplifying said subtractor output to generate said input signal for a next one of said plurality of stages, wherein said sample is provided as said input signal for the

first one of said plurality of stages.

13. The device of claim 12, wherein said sub-ADC comprises said resistor ladder and said current source.

14. The device of claim 12, wherein said ADC operates in a differential mode.

15. The device of claim 12, wherein said ADC operates in a single-ended mode.

16. The device of claim 12, wherein said device comprises a wireless base station, said device further comprising:

an antenna receiving an external signal; and

an analog processor processing said external signal to generate said analog signal.

17. An integrated circuit for applying a desired voltage at a first node, said first node being coupled to a load impedance, said integrated circuit comprising:

a voltage path connecting a voltage source to said first node, said voltage source providing said desired voltage; and

a current path connecting a current source to said first node, wherein said current source supplies an amount of current that would be approximately drawn by said load impedance if said desired voltage were to be applied at said first node.

18. The integrated circuit of claim 17, wherein said load impedance is characterized

by a high load such that said current source enables said voltage source to be coupled to said first node without a buffer between said voltage source and said first node.

19. The integrated circuit of claim 17, wherein said desired voltage is to be applied to a plurality of nodes including said first node, said plurality of nodes being connected in series with a corresponding routing resistance present between each pair of said plurality of nodes, each of said plurality of nodes being connected to a corresponding one of a plurality of load impedances, said integrated circuit further comprising:

a plurality of current paths, each coupling a corresponding one of a plurality of current sources to a corresponding one of said plurality of nodes, each of said plurality of current sources supplying an amount of current approximately equal to said desired voltage divided by an impedance driven by the corresponding coupled node, said plurality of current sources comprising said current source and said plurality of current paths comprising said current path.

20. The integrated circuit of claim 17, wherein said integrated circuit operates in a differential mode.